Amendments to the Drawings:

The attached sheets of drawings include changes to Fig. 1A, Fig. 1B, Fig. 1C and Fig. 3. These sheets, which include only Fig. 1A, Fig. 1B, Fig. 1C and Fig. 3 replace the original sheets including Fig. 1A, Fig. 1B, Fig. 1C and Fig. 3.

Attachment: Replacement Sheets 1/10, 2/10, 3/10 and 5/10.

REMARKS

The applicant appreciates the Examiner's thorough examination of the Application and requests reexamination and reconsideration of the Application in view of the following remarks.

As a preliminary matter, the applicant proposes amendments to the drawings. The proposed amendments include correcting the typographical error "data from tune path" to "data from func. path" indicated on Fig. 1A, Fig. 1B, and Fig. 1C. No new matter has been added. The amendments to Fig. 3 include adding reference number 80 to the dashed line between MBIST controller 62 and User Programmable Data Pattern Register 70. Reference number 89 has also been added to the line between Switch 88 and User Programmable Data Pattern Register 70. These reference numbers were inadvertently not included in the formal drawings filed on June 1, 2004, but were included in the drawings with the application as filed. Support for reference numbers 80 and 89 is found in the applicant's specification on page 12, lines 7-13. No new matter has been added.

The Examiner rejects claims 1-17 under 35 U.S.C. §102(e) as being anticipated by Ross *et al.* (U.S. Patent Application No. 2004/0190331).

The applicant's claimed universally accessible fully programmable memory built-in self-test (MBIST) system as recited in claim 1 includes: 1) an MBIST controller including an address generator configured to generate addresses for a memory under test, a sequencer circuit configured to deliver test data to selected addresses of the memory under test and reading out that test data, a comparator circuit configured to compare the test data read out of the memory under test to the test data delivered to the memory under test to identify a memory failure, and an externally accessible user programmable pattern register for

providing a pattern of test data to the memory under test; and 2) an external pattern programming device configured to supply the pattern of test data to the user programmable pattern register. Independent claims 16 and 17 recite similar features.

The innovative design of the universally acceptable fully programmable memory MBIST system of the applicant's claimed invention eliminates the need to hardwire logic for test data patterns, store the test patterns in ROM, or utilize algorithmic generation techniques to create test data patterns. Hardwired logic, ROM and algorithmic generation techniques all require the test data patterns or background patterns to be pre-programmed or pre-generated internally in the MBIST controller. The system and method of the applicant's invention as claimed relies on an externally accessible user programmable pattern register to provide a pattern of test data to the memory under test and an external pattern programming device that supplies the pattern of test data to the user programmable pattern register. The external pattern programming device, e.g., a computer or programmable hardware can supply a user defined pattern of test data to the externally accessible user programmable pattern register program provides for any user defined pattern of test data to be generated. The result is the elimination of the need to hardwire logic for test data patterns, utilize ROM to store numerous test data patterns, or use algorithmic generation techniques to generate fixed number of test data patterns. The system can be reconfigured and externally programmed to produce virtually any desired pattern of test data. Because the user defined pattern of test data is provided by an external programming device and is sent to the user programmable pattern register which is processed or transferred to the memory under test via the sequencer, the MBIST system of the applicant's invention can operate at the same speed as the memory under test. The user programmable data pattern register may be

external to the MBIST controller engine. *See* Fig. 3 of the applicants' specification and also page 12, lines 7-10, which recites:

> Although as shown in Fig. 3, user programmable pattern register 70 is located internal to MBIST controller 62, this is not a necessary limitation of this invention, as user programmable pattern register 70 may also be located external to MBIST controller 62, as indicated by dashed line 80.

In contrast, Ross *et al.* teaches and discloses an MBIST system that clearly utilizes hardwired input logic and output logic to generate the desired test data patterns: "typically, the circuit 100 also comprises input logic 120 and output logic 124 that can be used, for example, to insert tri-state drivers to drive busses..." *See* paragraph 45 of Ross *et al.* *See* also Fig. 1 of Ross *et al.* application which clearly shows input logic 120 and output logic 124. The finite state machine (FSM) as disclosed by Ross *et al.* is also clearly within and part of MBIST controller 104, as shown in Fig. 1 and not externally accessible.

Moreover, Ross *et al.* clearly discloses and teaches utilizing conventional MBIST controller technology to generate a test pattern using the input logic:

> According to some embodiments of the disclosed technology, a conventional MBIST controller for producing conventional test patterns is used. Fig. 2, for example, shows an embodiment of the modified MBIST architecture using a conventional MBIST controller. In order to use a conventional MBIST controller and conventional test patterns, the test values V that are input into the embedded memory 202 after the input logic 216 (F_1) are desirably identical to the test values output from the MBIST controller 204. (paragraph 56 of Ross *et al.*)

More proof of Ross *et al.*'s disclosing input logic is also disclosed in paragraph 46 as follows:

> Adjacent to the memory 202 are the memory's input logic 216 and output logic 218, as well as one or more input scan cells 220 and one or more output scan cells 222. The exemplary circuit shown in Fig. 2 may additionally comprise compensatory input logic 224 and compensatory output logic 226, which is described in greater detail below.

Ross *et al.* also teaches and discloses an MBIST system which is completely different from the applicant's claimed universally accessible fully programmable MBIST system and method as recited in independent claims 1, 16 and 17. Ross *et al.* teaches utilizing a scan cell that includes a sequential element, e.g., a flip-flop and a multiplexer placed in the data input path. The scan cell forms one of more serially connected chain of sequential elements that allow for loading and unloading of scan-chain data.

In contrast, as discussed above, the applicants claim universally accessible fully programmable MBIST system includes an MBIST controller with an address generator that generates an address for the memory under test, a sequencer circuit that delivers the test data to selected addresses of the memory under test and reads out the test data, a comparator circuit that compares the test data read out of the memory under test to the test data delivered to the memory under test to identify a memory failure, an externally accessible user programmable pattern register that provides a pattern of test data to the memory under test, and an external pattern programming device that supplies the pattern of test data to the user programmable pattern register.

Therefore, for the reasons stated above, Ross *et al.* clearly does not teach, suggests, or disclose each and every element of the applicants' invention, namely an externally accessible user programmable pattern register that provides a pattern of test data to the memory under test and an external pattern programming device configured to supply the pattern of test data to the user programmable register. Accordingly, independent claims 1, 16 and 17 are clearly allowable and patentable under 35 U.S.C. §102(e) over Ross *et al.* Because claims 2-15 depend from allowable claims, claims 2-15 are clearly patentable under 35 U.S.C. §102(e) over Ross *et al.*

If for any reason this Response is found to be incomplete, or if at any time it appears that a telephone conference with counsel would help advance prosecution, please telephone the undersigned, or his associates, collect in Waltham, Massachusetts, at (781) 890-5678.

Respectfully submitted,

Roy J. Coleman
Reg. No. 48,863